**CSCE/EE A241 Section 252: Computer Hardware Concepts**

**Spring 2022**

**CRN 37744/32936**

Zoom Lecture Schedule: 10:00 – 11:15 AM TR

Instructor: Frank W. Moore, Professor and Chair

Office: Zoom

E-mail: fwmoore@alaska.edu

Office Hours: 11:30 AM – 1:00 PM TR

or by email

or by appointment

NOTE: Students must be simultaneously enrolled in a lecture section and one of the four laboratory sections.

“Lab” Schedule:

CRN 32605/32938: CSCE/EE A241L 252: 1:00 – 2:15 PM TR

Tutor: TBD

CRN 32606/32939: CSCE/EE A241L 253: 2:30 – 3:45 PM TR

Tutor: Macklen Bell (Discord: MDawg25#7137; Email: [mibell@alaska.edu](mailto:mibell@alaska.edu))

Additional tutoring hours will be announced soon.

Textbook: Mano, M. and M. Ciletti 2017. *Digital Design*: *With an Introduction to the Verilog HDL, VHDL, and SystemVerilog* (6th Ed.), Pearson Education, Inc. ISBN-13 978-0134549897.

Grading: 25% First Midterm

25% Second Midterm

25% Final Exam

25% Homework (replaces Laboratory)

Course Description (Adjusted for COVID-19):

Design of digital systems. Topics include switching algebra and switching functions, design of combinational and sequential circuits using TTL, combinational logic design with MSI and LSI, flip-flops, registers, counters, register-level design, and algorithmic state machines. Students must show competency in the design of digital systems. CSCE/EE A241is a 4-credit course with 3 hours lecture and 3 hours laboratory.

Student Learning Outcomes (Adjusted for COVID-19):

Students will learn principles of digital systems design. They will use classic methodologies to design and document digital systems. Each student will ultimately be able to:

1. Analyze a given combinational or sequential circuit, producing an appropriate truth table or state table and state diagrams.
2. Create an appropriate state table and state diagrams to satisfy all system specifications.
3. Design combinational and sequential circuits to satisfy functional specifications of moderate complexity.
4. Predict the timing behavior of combinational and sequential systems.
5. Use accepted standards to document sequential logic designs.

Laboratory Description (Adjusted for COVID-19):

Due to COVID-19, “laboratories”, in the traditional sense, will once again *not* be held this semester. Instead, lab instructors will hold online tutoring hours during the regularly scheduled lab sessions and additional tutoring hours (TBD). Their job isn’t to do your homework assignments for you; instead, they are there to help you better understand concepts and design techniques, so that you can do the assignments yourself!

Disability Support Services:

If you need disability-related accommodations, please notify me and contact UAA Disability Support Services (RH 112, 786-4530) as soon as possible.

Course Web Access:

All of the materials discussed in this course are available on Blackboard (<https://classes.alaska.edu/>). Use your UAA user name and password to login. If you need help with Blackboard, training is available.

Attendance:

Past experience has demonstrated that regular attendance is essential to attaining a clear understanding of the subject matter. Many lectures will use example problems and supplementary material not explicitly provided by the textbook or notes.

Notes:

1. UAA’s definition of academic dishonesty may be found on its web site. This semester, students are strongly encouraged to study together, as well as to seek assistance from the instructor and/or lab instructors during scheduled office and lab hours and tutoring sessions. However, all work (exams and homework) submitted for this class must be completed individually by each student, without assistance from any other person. Any student suspected of academic dishonesty will be referred to the Dean of Students; *if found guilty, that student will earn an F in this course*.

2. Exams will be open book, open notes, open e-book, and open e-notes.

Detailed Course Schedule (subject to modification if necessary):

1/11 (T) Lecture 1A: Introduction, Number Bases

1/13 (R) Lecture 1B:Complements, Binary Numbers, Binary Codes, Binary Logic and Gates

1/18 (T) Lecture 2A: Boolean Algebra and Boolean Functions

1/20 (R) Lecture 2B: Canonical and Standard Forms

1/25 (T) Lecture 3A: Digital Logic Gates and Integrated Circuits

1/27 (R) Lecture 3B: Karnaugh Maps

2/01 (T) Lecture 4A: POS, SOP, Don’t-Care Conditions

2/03 (R) Lecture 4B: Two-Level Implementations, Exclusive-OR

2/08 (T) Lecture 5A: Review

2/10 (R) Lecture 5B: **First Midterm**

2/15 (T) Lecture 6A: Analysis and Design of Combinational Circuits

2/17 (R) Lecture 6B: Binary Adder/Subtractor

2/22 (T) Lecture 7A: Adders, Multipliers, Comparators

2/24 (R) Lecture 7B: Decoders, Encoders

3/01 (T) Lecture 8A: Multiplexers

3/03 (R) Lecture 8B: Sequential Circuits, Latches, Flip-flops

3/15 (T) Lecture 9A: Clocked Sequential Circuits

3/17 (R) Lecture 9B: State Reduction and Assignment

3/22 (T) Lecture 10A: Sequential Design using JK and D Flip-flops

3/24 (R) Lecture 10B: Review

3/29 (T) Lecture 11A: **Second Midterm**

3/31 (R) Lecture 11B: Registers, Shift Registers

4/05 (T) Lecture 12A: Ripple Counters, Synchronous Counters

4/07 (R) Lecture 12B: RTL, Algorithmic State Machines

4/12 (T) Lecture 13A: Binary Multiplier

4/14 (R) Lecture 13B: Control Logic

4/19 (T) Lecture 14A: Review

4/21 (R) Lecture 14B: TBD

4/26 (T) **Final Exam**, 10:00 AM – 12:45 PM